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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,364	10/11/2001	Edwin Park	TI-31696	9521

23494 7590 03/21/2005

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EXAMINER	
KNAPP, JUSTIN R	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,364	PARK, EDWIN	
	Examiner	Art Unit	
	Justin Knapp	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 7 is rejected under 35 U.S.C. 112, second paragraph. Claim 7 recites the limitation "the state machine" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-23 are rejected under 35 U.S.C. 102(a) as being anticipated by Nilsson et al (hereby Nilsson), USPN 6,189,052.

Referring to claim 1, Nilsson teaches:

a controller (figure 1, #2);

a configuration database coupled to the controller, said configuration database having stored therein a plurality of different configuration protocols for supporting a plurality of different peripheral devices (col 14, lines 29-31 teach a variety of protocols are supported);

a plurality of interconnection pads (figure 1, #6); and

a memory coupled to the interconnection pads and controller, the memory is programmable by the controller in order to support any of the different peripheral devices (figure 3, #19, column 7).

Referring to claim 2, Nilsson teaches wherein the controller comprises a state machine (figure 1, #2 is a state machine).

Referring to claim 3, Nilsson teaches a multiplexer coupled between the memory and the plurality of connection pads (column 10 teaches configuration logic with select circuitry for a plurality of pins).

Referring to claim 4, Nilsson teaches a programmable clock coupled to the memory or the configuration database (figure 2, #26).

Referring to claim 5, Nilsson teaches wherein the controller selects a configuration protocol from amongst the plurality of configuration protocols in the configuration database, and uses the selected configuration protocol to configure the memory in order to support the peripheral device from amongst the plurality that is coupled to the plurality of interconnection pads (configuration logic, #5 makes it possible to share i/o pins between different protocols, column 3).

Referring to claim 6, Nilsson teaches wherein the state machine includes a programmable routing and mapping scheme that allows the state machine to communicate with more than one peripheral device that is coupled to the plurality of interconnection pads (figure 2 shows the i/o processor able to map and route a variety of protocols from different peripherals, column 6).

Referring to claim 7, Nilsson teaches wherein the state machine can control the programmable clock so that it generates the necessary clock patterns required by the peripheral device coupled to the plurality of interconnection pads (figure 2, has special timers, #26, that can generate necessary clock patterns).

Referring to claim 8, Nilsson teaches wherein the memory can be divided up by the state machine into two or more parts in order to support a peripheral device coupled to the interconnection pads that requires continuous transfer of data, the state machine switching between the two or more parts of the memory during data transfer to the peripheral device (column 5, line 35-end).

Referring to claim 9, Nilsson teaches wherein the state machine sets a portion of the memory to provide a tri-state control if one or more of the plurality of interconnection pads have to function as both an input and an output (column 10, line 30 and column 13, lines 50-62).

Referring to claim 10, Nilsson teaches a method for interfacing a controller with an electronic peripheral device that utilizes a predefined communications protocol, comprising the steps of:

selecting the appropriate configuration protocol for use with the electronics peripheral device from amongst a plurality of configuration protocols (an i/o processor, figure 1, 2, with its configuration logic, #5 selects the appropriate configuration protocol);

providing a memory (figure 3, #19) ; and

selectively interconnecting conductive pads coupled to the electronic peripheral device with sections of the memory programmed to support the configuration protocol used by the electronic peripheral device (figure 2, #6 and 29 control the pins).

Referring to claim 11, Nilsson teaches receiving signals from the electronic peripheral device upon the conductive pads, and responsive thereto performing device-output-processing operations comprising:

directing the signals from the pads to the memory (register bank, figure 3, #19 stores signals); and

storing the signals in the memory (as taught above).

Referring to claim 12, Nilsson teaches receiving signals to be sent to the electronic peripheral device and responsive thereto performing output signal processing operations comprising:

loading the output signals into the memory (column 7); and

outputting the output signals from memory with timing compliant with the identified communications protocol (signals output from processor, figure 2, #2 with timing provided by timers, #26).

Referring to claim 13, Nilsson teaches a method for universally interfacing a processor with an electronic peripheral device that utilizes a communications protocol of a prescribed list of multiple communications protocols, comprising operations of:

detecting that a peripheral device is coupled to the processor (peripheral devices, figure 1, #13-15 are detected by processor, #2, with configuration logic #5) ;

identifying the communication protocol used by the peripheral device coupled to the processor from a list of protocols supported by the processor (processor, #2, handles this function);

receiving identification of first communications protocols utilized by a first peripheral device coupled to multiple conductive pads (processor, #2, identifies peripherals coupled to pins #6); and

selectively interconnecting the pads with memory input lines pursuant to the identified communications protocol (register bank, figure 3, #19 receives corresponding protocol signals from selected pins).

Referring to claim 14, Nilsson teaches a method further comprising the steps of:

receiving output signals from the peripheral device upon the conductive pads, and responsive thereto performing device-output-processing operations comprising:

directing the output signals from the pads to the memory via the pads and memory input lines;

storing the output signals in the memory; and

directing the memory to output stored signals to the processor (see rejection of claim 11).

Referring to claim 15, Nilsson teaches:

receiving processor output signals from the processor and responsive thereto performing processor output processing operations comprising:

loading the processor output signals into the memory; and outputting the processor output signals from memory with timing compliant with the identified communications protocol (see rejection of claim 12).

Referring to claim 16, Nilsson teaches where the peripheral device comprises multiple peripheral devices, and the operations further comprising time-dividing utilization of the pads between the multiple peripheral devices (configuration logic supports multiple protocols at once, column 3, lines 1-6 and special timers, figure 2, #26 provide time-dividing utilization).

Referring to claim 17, Nilsson teaches where:

the operations further include receiving identification of a second communications protocol different than the first communication protocol (configuration logic supports multiple protocols at once, column 3, lines 1-6);

responsive to receiving the identification of the second communication protocol, conducting the processor-output-processing operations according to the second communications protocol (processor, #2, handles multiple protocols and conducts appropriate operations as taught above).

Referring to claim 18, Nilsson teaches a method of interfacing a processor with a peripheral device having one of multiple predetermined types, each type of peripheral device being designed to operate according to a different predefined communications protocol, comprising operations of:

providing an interface apparatus including a controller, memory, and multiple input/output nodes (figure 1, #2);

the controller receiving notification of presence of a peripheral device coupled to the input/output nodes, including the type of the peripheral device (figure 1, #2, processor receives presence of peripheral devices via pins, #6); and

responsive to the presence of the peripheral device, the controller operating the memory to simulate behavior of a dedicated interface between the processor and the peripheral device coupled to the input/output nodes (figure 1, #2 has a variety of memory banks and registers such as figure 3, #19 to simulate behavior between the processor and the peripheral devices coupled to pins #6).

Referring to claim 19, Nilsson teaches:

recognizing by the controller any changes in peripheral device type coupled to the input/output nodes, and responsive to such changes the controller operating the memory to simulate behavior of a dedicated interface corresponding to the changed peripheral device (processor #2, column 9, lines 47-55).

Referring to claim 20, Nilsson teaches a method operating a universal interface which can support a plurality of communication protocols and including a multiplexer interposed between a memory and multiple input/output pads, the method comprising operations of:

identifying a communication protocol from amongst the plurality of communication protocols applicable to a peripheral device attached to the input/output pads (as taught herein above);

retrieving pre-stored operating parameters corresponding to the identified communications protocol (column 9 line 55 through column 10); and

configuring the multiplexer to selectively couple the input/output pads to the memory with mapping specified by the operating parameters ((column 10 teaches configuration logic with select circuitry for a plurality of pins).

Referring to claim 21, Nilsson teaches configuring a clock to provide a reference signal having a frequency specified by the operating parameters required by the identified communication protocol (figure 6 and special timers, figure 2, #26).

Referring to claim 22, Nilsson teaches loading data form a state machine into the memory; and transmitting data from the memory to the pads via the multiplexer (column 10).

Referring to claim 23, Nilsson teaches receiving data from the peripheral device into the memory via the multiplexer (column 10).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin Knapp whose telephone number is (571)272-4149. The examiner can normally be reached on Mon - Fri 8:30 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on (571)272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin Knapp
Examiner
Art Unit 2182

March 13, 2005

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
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